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None

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INT CL^5 H01L

(54) Semiconductor device comprising ferroelectric capacitor

(57) In a semiconductor device having a ferroelectric capacitor and manufacturing method therefor, a spacer (60) comprising a low dielectric material is formed on the side surfaces of a plurality of lower electrodes (35) separated into each of a plurality of cell units to prevent an error which may be caused between the adjacent lower electrodes. A ferroelectric film (40) is formed on the lower electrodes whereon the low dielectric material spacer is formed, and an upper electrode (50) is formed on the ferroelectric film. The semiconductor device can be a dynamic random access memory device (DRAM).

FIG. 8

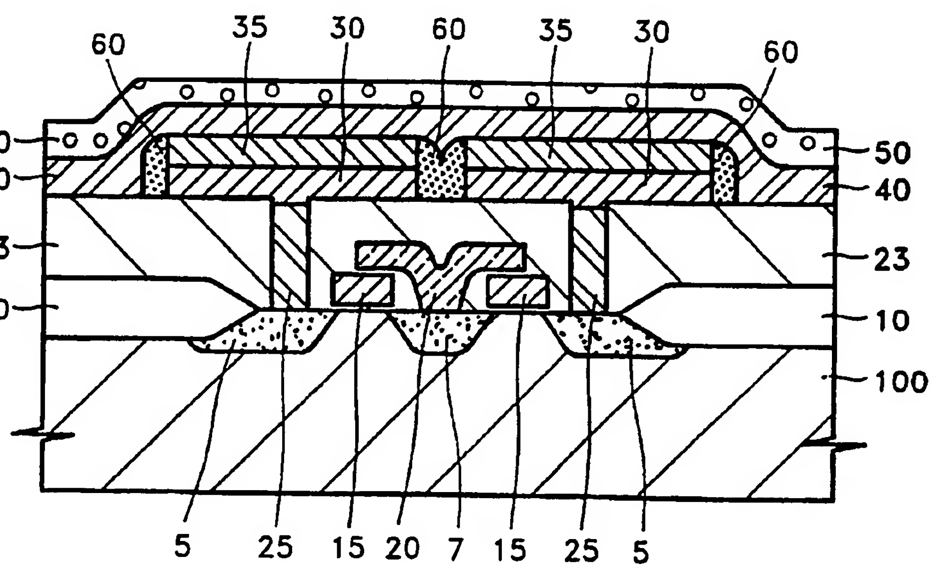

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FIG. 1(PRIOR ART)

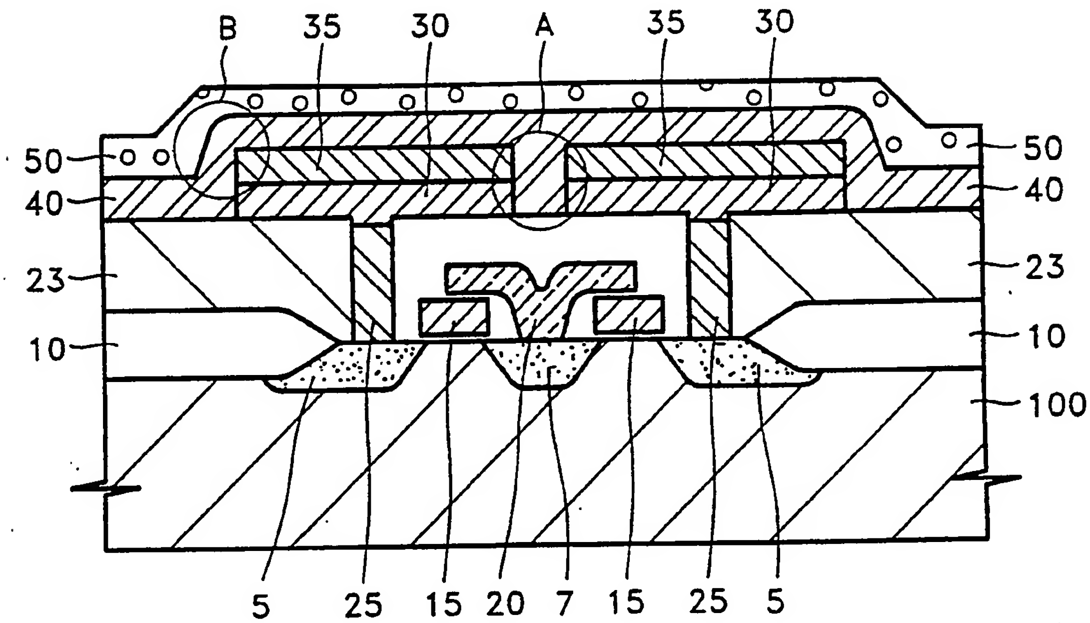


FIG. 2A(PRIOR ART)

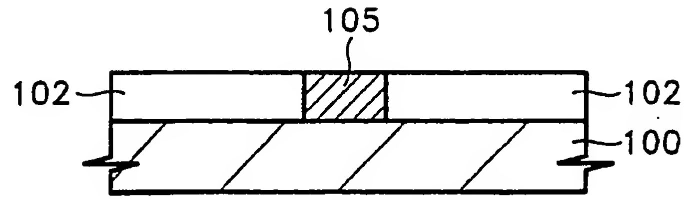


FIG. 2B(PRIOR ART)

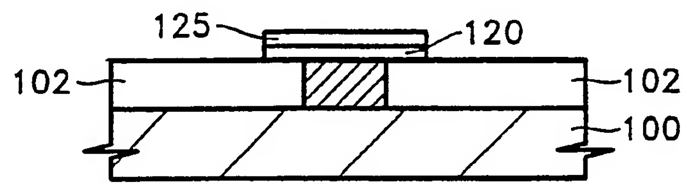


FIG. 2C(PRIOR ART)

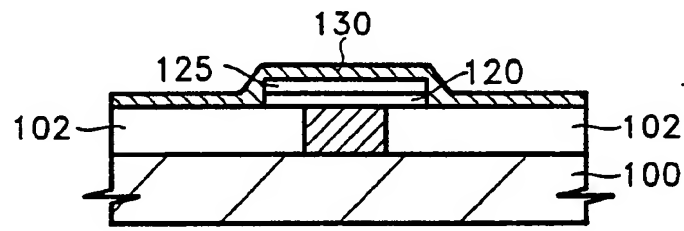


FIG. 2D(PRIOR ART)

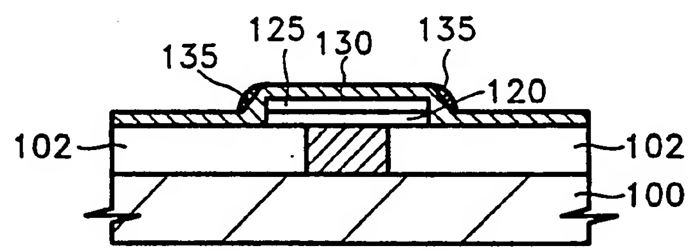


FIG. 2E(PRIOR ART)

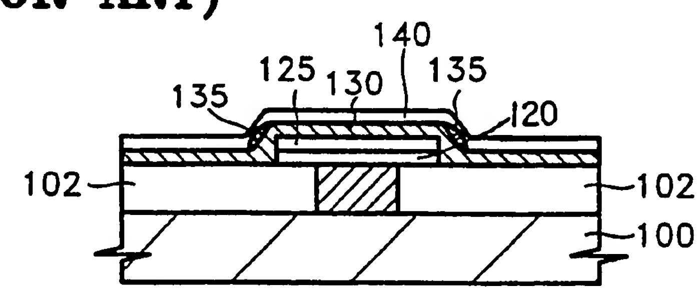


FIG. 3

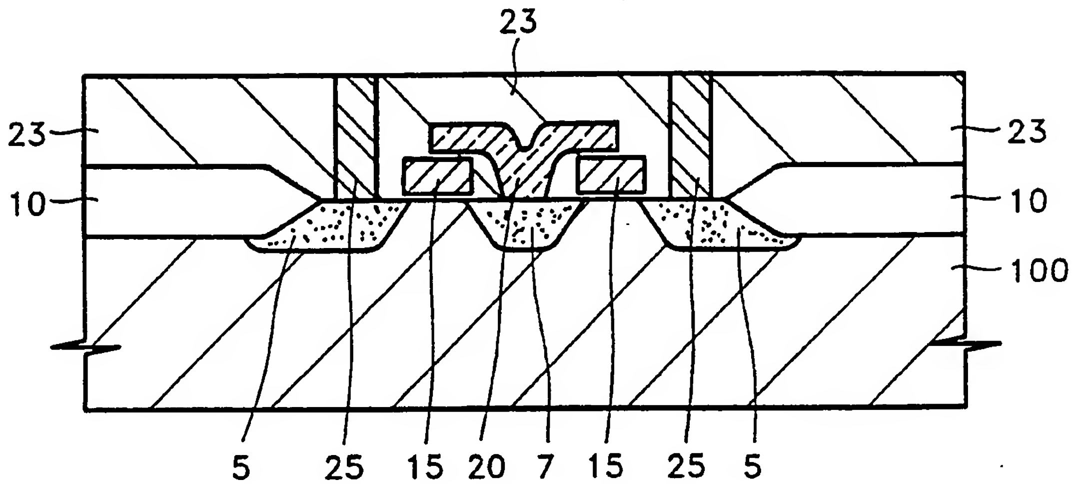

23
23
23
10
10
100
5
25
15
20
7
15
25
5

FIG. 4

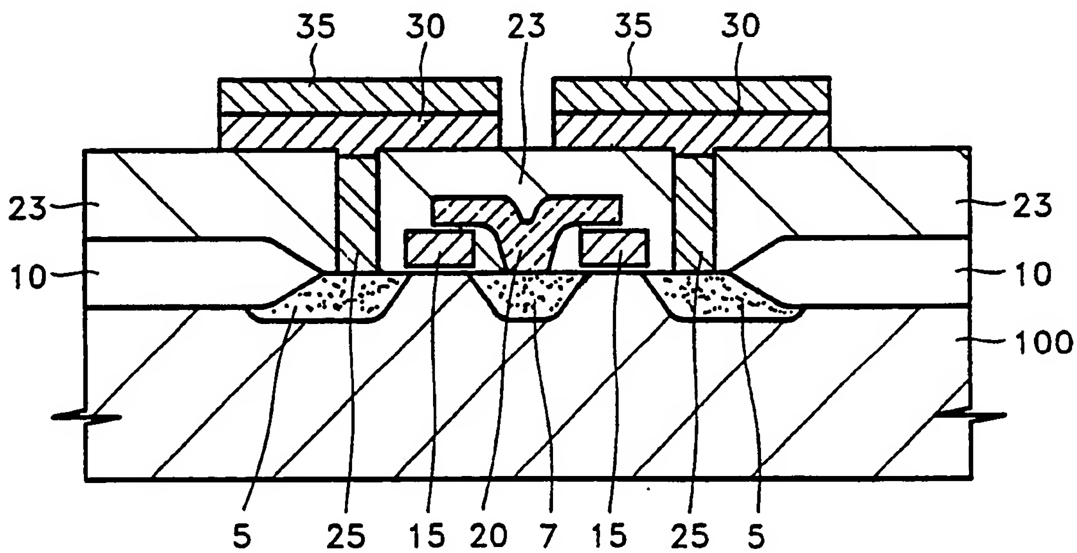

35
30
23
35
30
23
23
10
10
100
5
25
15
20
7
15
25
5

FIG. 5

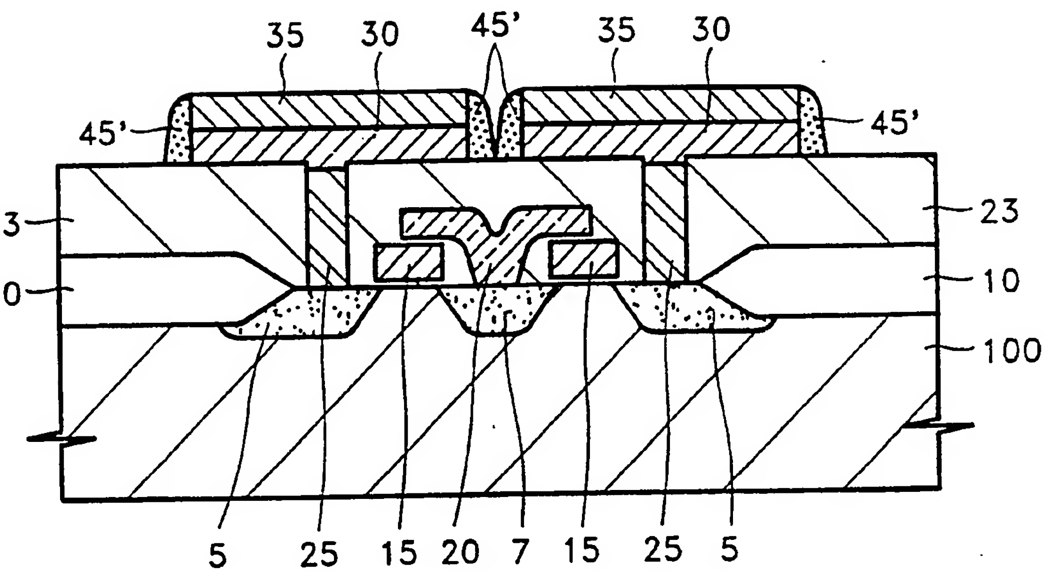
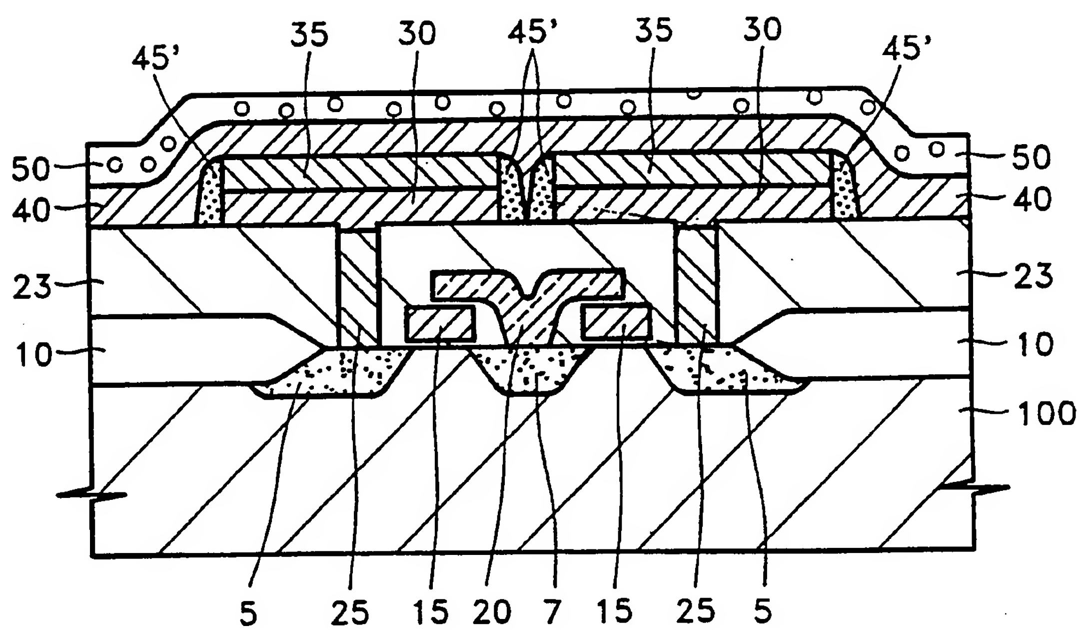

35
30
45'
35
30
45'
45'
23
23
10
10
100
5
25
15
20
7
15
25
5

FIG. 6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35
30
45'
35
30
45'
50
50
40
40
23
23
10
10
100
5
25
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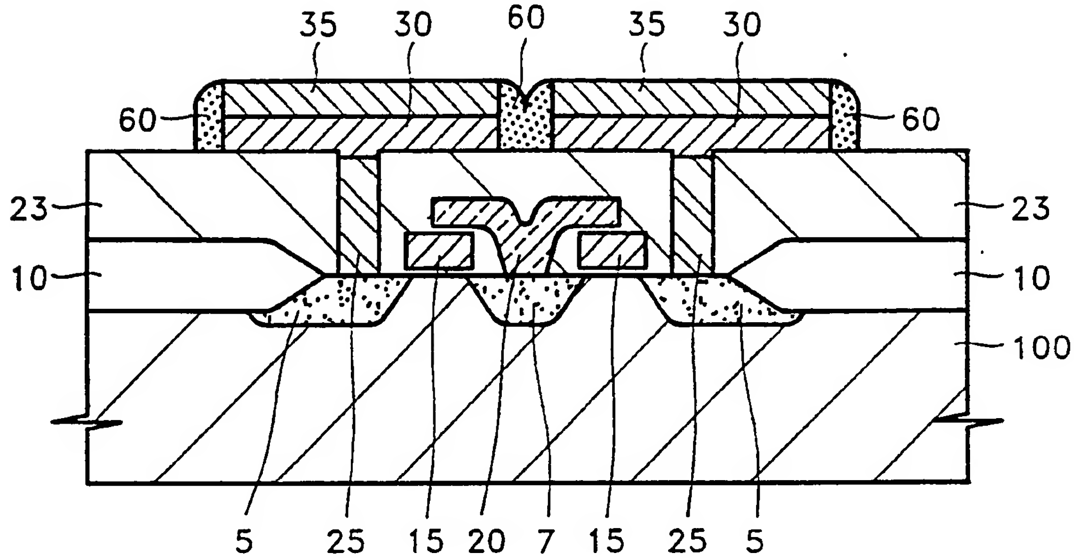
20
7
15
25
5

FIG. 7


35
30
60
35
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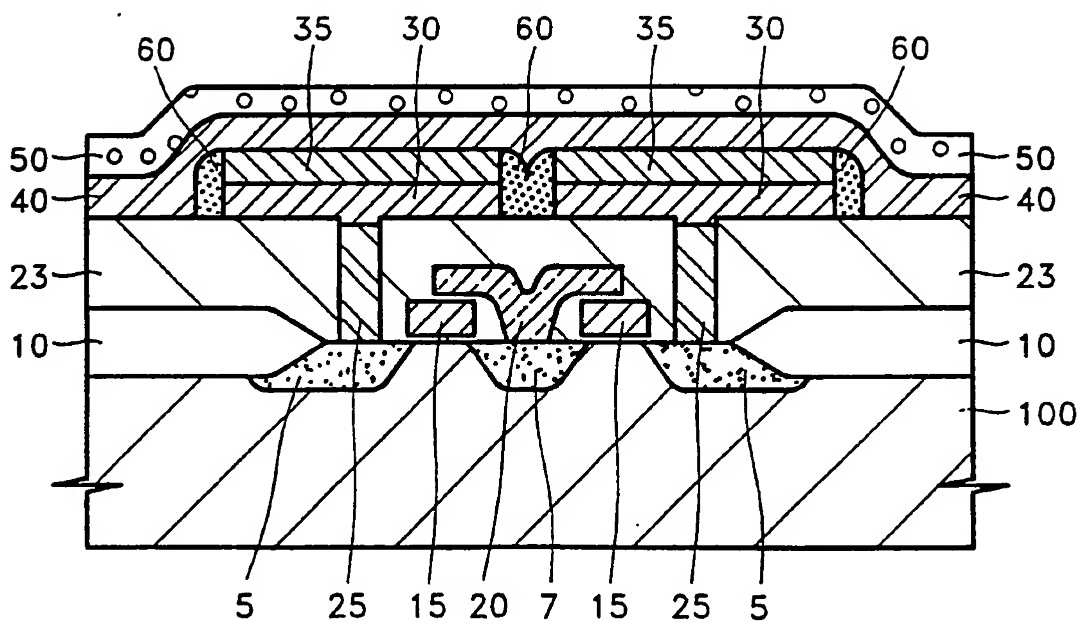
60
60
23
23
10
10
100
5
25
15
20
7
15
25
5

FIG. 8


60
35
30
60
35
30
60
50
50
40
40
23
23
10
10
100
5
25
15
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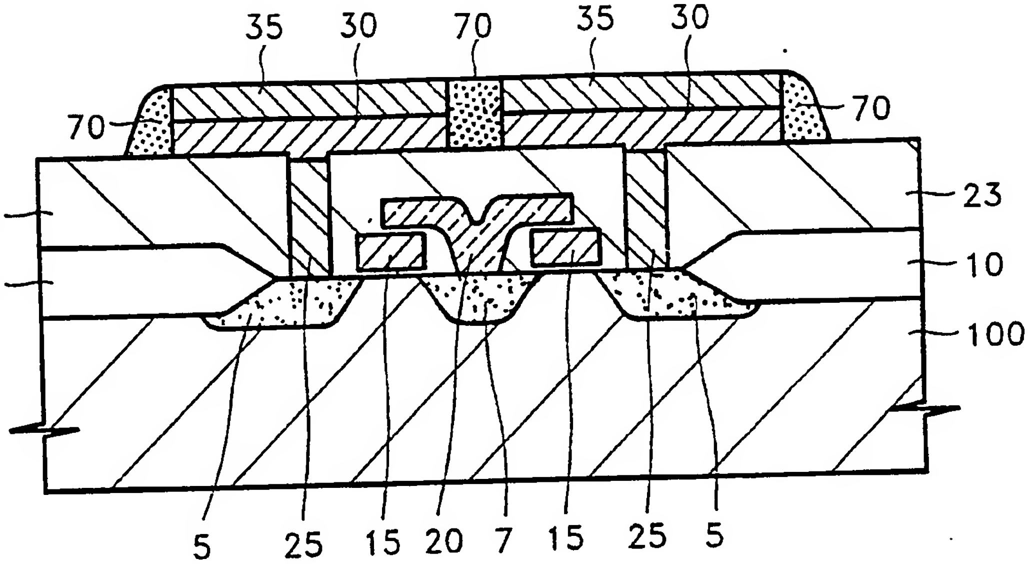
7
15
25
5

FIG. 9


35
30
70
35
30
70
70
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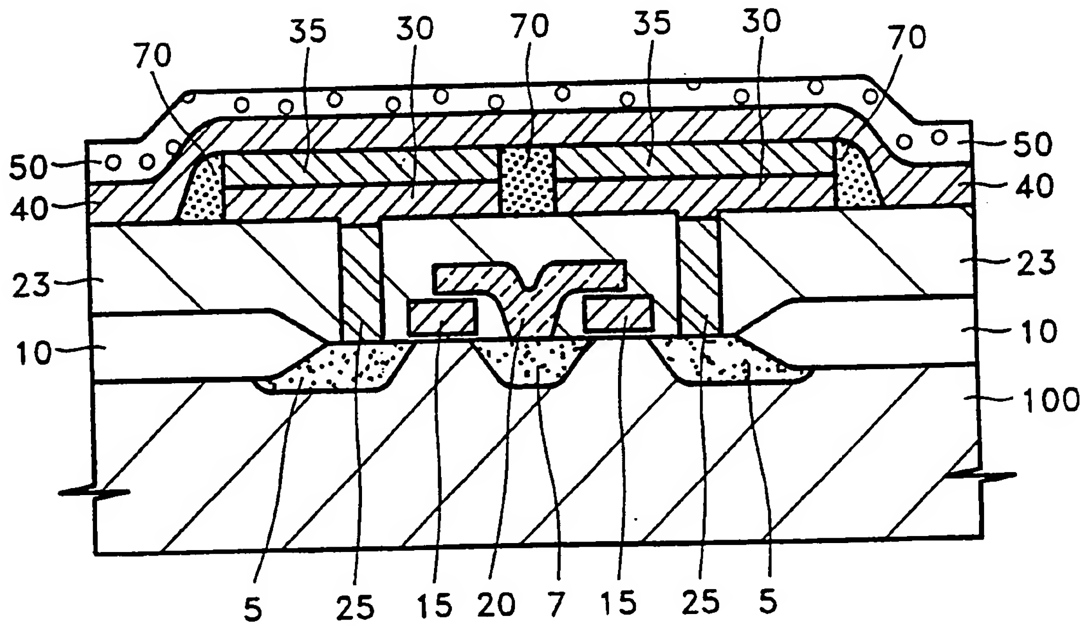
10
23
10
100
5
25
15
20
7
15
25
5

FIG. 10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30
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35
30
70
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40
23
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50
40
23
10
100
5
25
15
20
7
15
25
5

SEMICONDUCTOR DEVICE AND METHOD FOR ITS MANUFACTURE

The present invention relates to a semiconductor device and a method for its manufacture in which a ferroelectric film is used as the dielectric film of a capacitor.

As the integration of dynamic random access memory (DRAM) devices increases, many methods for increasing capacitance within the limited cell area are proposed. These methods can be largely divided into two groups: a method in which a capacitor structure is improved and a method in which a material having a high dielectric constant is used.

As a method for improving capacitor structure, there is a method in which the effective area of the capacitor is increased by forming a three-dimensional storage electrode. Here, however, design rule limitations and a complicated manufacturing process impede the increase in capacitance.

By contrast, the method in which a material having a high dielectric constant is used as the dielectric film of the capacitor, is not limited by design rule. Therefore, capacitance can be easily increased.

Recently, a method in which a ferroelectric material is used as the dielectric film has been proposed. Unlike the existing oxide, silicon nitride or tantalum pentoxide (Ta_2O_5) films, a ferroelectric material is a material which exhibits spontaneous polarization, and generally has a dielectric constant of at

least 1,000. When the ferroelectric material is used as the dielectric film, the thickness of an equivalent oxide film can be made thin, for example, 10Å or less, even though the ferroelectric material is formed to a thickness of only several thousand angstroms. Furthermore, due to the spontaneous polarization phenomenon, an dielectric film using a ferroelectric material can be used for nonvolatile memory devices as well as for DRAMs.

In addition, PZT ($PbZrTiO_3$), BST ($BaSrTiO_3$) and the like have a high dielectric constant and their ferroelectric characteristics differ according to the composite ratio, and therefore, have recently been popular as dielectric materials for DRAM capacitors. When such materials are used for the dielectric film, platinum is used as the electrode material of the capacitor, due to its great resistance to oxidation.

FIG.1 of the accompanying drawings is a sectional view of a semiconductor device having a ferroelectric film capacitor manufactured by the conventional method.

Referring to FIG.1, a transistor pair is formed in the active region defined by field oxide film 10 of a semiconductor substrate 100. The transistors share a drain region 7 and each comprises a source region 5 and a gate electrode 15. A bit line 20 is connected to drain region 7, and contact holes for exposing the predetermined portions of each source region 5 are formed.

Each contact hole is filled with a conductive plug 25 and the

capacitors' lower electrodes, each consisting of a titanium layer 30 and platinum layer 35, are formed on each plug. A ferroelectric thin film 40 is formed over the lower electrodes, and an upper electrode 50 is formed on ferroelectric thin film 40.

In a capacitor manufactured according to the conventional method described above, the film can be weakened at the sharp edge of the lower electrode (see area "B" of FIG.1), when the ferroelectric film is formed after lower electrode formation. In addition, since the dielectric constant of a ferroelectric film is very high, roughly from 1,000 to 10,000, there is a high possibility for causing an error between the adjacent capacitors through the ferroelectric film which exists between the adjacent lower electrodes (see are "A" of FIG.1).

In 1991, Kuniaki Koyama et al. disclosed a new method for manufacturing a capacitor in order to solve the problems described above (see IEDM '91, "A Stacked Capacitor with $(Ba_xSr_{1-x})TiO_3$ for 256M DRAMs").

FIGs.2A to 2E of the accompanying drawings are sectional views for illustrating a method for manufacturing the capacitor.

Referring to FIG.2A, an insulating layer 102 is formed on semiconductor substrate 100, and a contact hole 105 is formed by etching a predetermined portion of insulating layer 102. Then, impurity-doped polysilicon is deposited all over the resultant structure. Then, the structure is etched back so that contact hole 105 remains filled with polysilicon.

Referring to FIG.2B, a tantalum layer and a platinum layer are sequentially sputtered on the resultant structure, each to a thickness of 500Å. Both layers are then patterned by a dry-etching process to form a platinum pattern 125 and a tantalum pattern 120, which constitute a lower electrode.

Referring to FIG.2C, $(Ba_{0.5}Sr_{0.5})TiO_3$ is deposited all over the resultant structure by RF magnetron sputtering, thereby to form a ferroelectric film 130 having a thickness of 700~2,000Å.

Referring to FIG.2D, a chemical vapor deposition (CVD) oxide film having a thickness of 1,000Å is formed all over the resultant structure. The structure is etched anisotropically, to thereby form a spacer 135 which reduces leakage current caused by the poor step coverage of ferroelectric film 103.

Referring to FIG.2E, a titanium nitride (TiN) layer 140 as an upper electrode having a thickness of 1,000Å is formed all over the resultant structure.

A capacitor manufactured by the above method forms a CVD oxide film spacer whose breakdown resistance is excellent in the weak portion of the ferroelectric film, thereby to have a very low leakage current and a stable breakdown resistance distribution.

However, due to the very high dielectric constant of the ferroelectric film, the possibility that an error can be caused between the adjacent capacitors still remains.

Accordingly, it is an object of the present invention to provide a reliable semiconductor device in which the occurrence of errors between adjacent capacitors is prevented.

It is another object of the present invention to provide a method for manufacturing a semiconductor device especially suitable for manufacturing the above semiconductor device.

According to the present invention there is provided a semiconductor device having a capacitor wherein a spacer comprising a low dielectric material is formed on the side surfaces of plural lower electrodes which are separated into each cell unit, a ferroelectric film is formed on the lower electrodes whereon the low dielectric material spacer is formed, and an upper electrode is formed on the ferroelectric film.

According to another aspect of the present invention, there is provided a method for manufacturing a semiconductor device having a capacitor, comprising the steps of:

forming a first conduction layer on a semiconductor substrate;

forming a plurality of lower electrodes separated into each cell unit by patterning the first conduction layer;

forming a spacer comprising a low dielectric material on the side surfaces of each lower electrode;

forming a ferroelectric film all over the resultant structure whereon the spacer is formed; and

forming an upper electrode on the ferroelectric film.

According to a further aspect of the present invention, there is provided a method for manufacturing a semiconductor device having a capacitor, comprising the steps of:

forming a first conduction layer on a semiconductor substrate;

forming a plurality of lower electrodes separated into each cell unit by patterning the first conduction layer;

filling the space between the lower electrodes with a low dielectric material;

forming a ferroelectric film all over the resultant structure; and

forming an upper electrode on the ferroelectric film.

Accordingly, a spacer consisting of a low dielectric material is formed between each lower electrode, thereby to prevent the occurrence of errors between the adjacent capacitors.

Embodiments of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

FIG.1 is a sectional view showing a semiconductor device comprising a ferroelectric film capacitor manufactured by the conventional method;

FIGs.2A to 2E are sectional views for illustrating a method for manufacturing a ferroelectric film capacitor manufactured by another conventional method;

FIGs. 3 to 6 are sectional views for illustrating a method for

manufacturing a semiconductor device comprising a ferroelectric film capacitor according to an embodiment of the present invention;

FIGs. 7 to 8 are sectional views for illustrating a method for manufacturing a semiconductor device comprising a ferroelectric film capacitor according to another embodiment of the present invention, and

FIGs.9 to 10 are sectional views for illustrating a method for manufacturing a semiconductor device comprising a ferroelectric film capacitor according to a further embodiment of the present invention.

FIG.3 shows the step of forming a contact hole and a conductive plug 25 on a semiconductor substrate 100 whereon a transistor pair is formed. Semiconductor substrate 100 is divided into an active region and a isolation region by field oxide film 10. A pair of transistors, each having a source region 5 and a gate electrode 15 and sharing a drain region 7 and a bit line 20 connected to the drain region, is formed on the active region of semiconductor substrate 100. Then, an insulating layer (not shown) is formed all over substrate 100. A planarization layer 23 is formed all over the resultant structure, in order to planarize the uneven surface of substrate 100 which is due to the formation of the transistors and bit line. Then, planarization layer 23 and the insulating layer, which are deposited on source region 5, are selectively etched to form a contact hole for connecting the lower electrode of the capacitor to the source region. As a conductive material, a phosphorous-doped polysilicon is then deposited on substrate 100

where the contact hole is formed, and then etched back such that the contact hole is filled with a conductive plug 25.

FIG.4 shows the step of forming the lower electrodes of a capacitor. A titanium layer having a thickness of approximately 500Å and a platinum layer having a thickness of 1,000Å are sequentially formed by a sputtering method all over the resultant structure formed with conductive plug 25. A photoresist pattern (not shown) is then formed on the platinum layer (upper layer) by coating, exposing and developing the photoresist so as to define each cell. Then, both layers are simultaneously etched using the photoresist pattern as a mask, thereby to form the capacitor's lower electrode which consists of platinum pattern 35 and titanium pattern 30. The first photoresist pattern is then removed. Here, tantalum can be used instead of titanium for constituting the lower electrode.

FIG.5 shows the step of forming a first spacer 45'. As a low dielectric material, plasma-enhanced SiO_2 (PE-SiO_2), a CVD oxide film, silicon nitride (Si_xN_y), boro-nitride (BN), boro-phosphorous silicate glass (BPSG), phosphorous silicate glass (PSG), undoped silicate glass (USG) or boro-silicate glass (BSG) is deposited to a thickness of 1,500Å to 2,000Å on the resultant structure whereon the lower electrode is formed. Then, the above low dielectric material is etched anisotropically to form first spacer 45' on the side surfaces of the lower electrode.

FIG.6 shows the step of forming a ferroelectric film 40 and an upper

electrode 50. As a ferroelectric material, PZT, $PbTiO_3$ (PLT), $PbLaZrTiO_3$ (PLZT), $SrTiO_3$ (STO), BST or $LiNbO_3$ (LNO) is deposited by a CVD method on the resultant structure whereon first spacer 45′ is formed, so that ferroelectric film 40 can be formed. Then, as a conductive material, platinum, TiN or aluminum is deposited on ferroelectric film 40 so as to form the capacitor's upper electrode.

FIGs.7 to 8 are sectional views for illustrating a method for manufacturing a semiconductor device comprising a ferroelectric film capacitor according to another embodiment of the present invention.

FIG.7 shows the step of forming the lower electrodes of the capacitor and a second spacer 60. After forming the lower electrodes using the method explained with respect to FIGs.3 and 4, as a low dielectric material, BN, BPSG, BSG or SiO_2 is deposited to a thickness of approximately 2,000Å to 10,000Å all over the resultant structure. Then, the low dielectric material is etched anisotropically so that second spacer 60 can be formed on the side surface of the lower electrodes which consist of platinum pattern 35 and titanium pattern 35. At this time, second spacer 60 is formed to fill the space between the adjacent lower electrodes.

FIG.8 shows the step of sequentially forming ferroelectric film 40 and upper electrode 50 on the lower electrodes on whose side surfaces are formed with second spacer 60, using the method explained with respect to FIG.6.

FIGs.9 and 10 are sectional views for illustrating a method for

manufacturing for a semiconductor device which comprises a ferroelectric film capacitor according to a further embodiment of the present invention.

FIG.9 shows the step of forming the lower electrodes and a third spacer 70. After forming the lower electrodes using the method explained with respect to FIGs.3 and 4, as a low dielectric material, BPSG, PSG or BSG is deposited to a thickness of approximately 2,000Å to 10,000Å all over the resultant structure. Then, the low dielectric material is planarized by a high-temperature heat treatment process, and the resultant structure is etched anisotropically, so that third spacer 70 can be formed on the side surfaces of the lower electrode which consists of platinum pattern 35 and titanium pattern 30. At this time, third spacer 70 has to completely fill up the space between the adjacent lower electrodes so that the lower electrodes of each cell can be separated by a planarized surface.

FIG.10 shows the step of sequentially forming ferroelectric film 40 and upper electrode 50 on the lower electrodes on whose side surfaces are formed with third spacer 70, using the method explained with respect to FIG.6.

As described above, according to embodiments of the present invention, a spacer consisting a lower dielectric material is formed on the side surfaces of a capacitor's lower electrode so that an error which may be caused between the adjacent lower electrodes can be prevented. The sharp edges of the lower electrodes are somewhat alleviated by the spacer. As a result, the possibility that the ferroelectric film may be weakened in the area of the sharp

edges can be prevented.

In addition, in all the above embodiments, since a spacer consisting of the low dielectric material is formed by a simple anisotropic etch process without any additional mask, the problems generated in the conventional method can be easily solved without processing problems and without increasing production costs.

It is understood by those skilled in the art that the foregoing description is a preferred embodiment of the disclosed device and that various changes and modifications may be made in the invention without departing from the scope thereof.

CLAIMS

1. A semiconductor device having a capacitor comprising:

a plurality of lower electrodes separated into each of a plurality of cell units;

a spacer comprising a low dielectric material formed on the side surfaces of said lower electrodes;

a ferroelectric film formed on said plurality of lower electrodes whereon said low dielectric material spacer is formed; and

an upper electrode formed on said ferroelectric film.

2. A semiconductor device according to claim 1, wherein said low dielectric material spacer is comprised of any one selected from the group consisting of PE-SiO_2, CVD oxide, Si_xN_y, BN, BPSG, PSG, USG and BSG.

3. A semiconductor device according to claim 1 or 2, wherein said low dielectric material spacer fills the space between said lower electrodes.

4. A semiconductor device substantially as herein described with reference to any of Figures 3 to 6 with or without reference to Figures 7 and 8 or Figures 9 and 10 of the accompanying drawings.

5. A method for manufacturing a semiconductor device having a

capacitor, comprising the steps of:

forming a first conduction layer on a semiconductor substrate;

forming a plurality of lower electrodes separated into each cell unit by patterning said first conduction layer;

forming a spacer comprising a low dielectric material on the side surfaces of each of the lower electrodes;

forming a ferroelectric film all over the resultant structure whereon said spacer is formed; and

forming an upper electrode on said ferroelectric film.

6. A method for manufacturing a semiconductor device having a capacitor, comprising the steps of:

forming a first conduction layer on a semiconductor substrate;

forming a plurality of lower electrodes separated into each of a plurality of cell units by patterning said first conduction layer;

filling the space between said lower electrodes with a low dielectric material;

forming a ferroelectric film all over the resultant structure; and

forming an upper electrode on said ferroelectric film.

7. A method for manufacturing a semiconductor device according to claim 6, wherein said space filling step comprises the steps of:

depositing a low dielectric material all over the resultant structure whereon said lower electrode is formed;

planarizing said low dielectric material; and

etching anisotropically said planarized low dielectric material.

8. A method for manufacturing a semiconductor device substantially as hereinbefore described with reference to Figures 3 to 6 with or without reference to Figures 7 and 8 or 9 and 10 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report)

-15-

Application number
GB 9401561.7

Relevant Technical Fields

(i) UK Cl (Ed.M) H1K (KFG, KFLS, KFLX, KGAMS, KGAMX)

(ii) Int Cl (Ed.5) H01L

Search Examiner
W A MORRIS

Date of completion of Search
30 MARCH 1994

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii)

Documents considered relevant following a search in respect of Claims :-
1-8

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

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